## IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

an isolation layer disposed in a semiconductor substrate, the isolation layer ~~defining an~~ defining an active region;

a gate pattern disposed on the active region;

source/drain regions disposed in the active region at both sides of the gate pattern;

sidewall spacers disposed on sidewalls of the gate pattern, the sidewall spacers comprising an inner spacer having an L-shaped cross-section that is formed on a sidewall of the gate pattern and neighboring the gate pattern, and an outer spacer having a cured sidewall that is formed on the inner spacer and covering entire sidewalls of the gate pattern;

a blocking insulation layer disposed on the isolation layer and on a portion of the active region neighboring the isolation layer, the blocking insulation layer spaced apart from the sidewall spacers; and

a first silicide layer disposed on the source/drain regions between the blocking insulation layer and the sidewall spacers and having a boundary aligned to edges of the blocking insulation layer and the sidewall spacer.

2. (Cancelled)

3. (Original) The semiconductor device of claim 1, wherein the isolation layer includes a dent at the region neighboring the active region, and

wherein the blocking insulation layer is formed on the dent.

4. (Previously presented) The semiconductor device of claim 1, further comprising a second silicide layer disposed on a top surface of the gate pattern.

5. (Withdrawn) A method of fabricating semiconductor devices comprising:

forming a isolation layer in a semiconductor substrate to define an active region;

forming a gate pattern on the active region;

implanting impurities into the active region at both sides of the gate pattern;

forming a spacer insulation layer on a surface of the semiconductor substrate with the gate pattern, the spacer insulation layer having a first region between the isolation layer and the gate pattern, wherein the closer the first region lies to the gate pattern, the thinner it becomes;

anisotropically etching the spacer insulation layer to form a sidewall spacer on a sidewall of the gate pattern, and to leave a blocking insulation layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

applying a silicidation process to the semiconductor substrate to form a silicide layer on a source/drain region between the blocking insulation layer and the sidewall spacer, the silicide layer having a boundary aligned to the edge of the blocking insulation layer and a boundary aligned to the edge of the sidewall spacer.

6. (Withdrawn) The method of claim 5, wherein forming the spacer insulation layer comprises:

stacking a silicon nitride layer and a silicon oxide layer, wherein the first region includes at least one of the silicon nitride layer and the silicon oxide layer.

7. (Withdrawn) The method of claim 6, wherein anisotropically etching the spacer insulation layer to form the sidewall spacer comprises:

anisotropically etching the silicon oxide layer to form an outer spacer having a curved sidewall on a side of a gate electrode; and

etching the silicon nitride layer using the outer spacer as an etch stop layer to form an inner spacer having an L-shaped cross-section between the outer spacer and the gate pattern.

8. (Withdrawn) The method of claim 5, wherein forming the spacer insulation layer comprises:

conformally forming a silicon nitride layer on the semiconductor substrate; and

forming a silicon oxide layer on the silicon nitride layer, wherein the first region comprises the silicon oxide layer.

9. (Withdrawn) The method of claim 8, wherein anisotropically etching the spacer insulation layer comprises:

anisotropically etching the silicon oxide layer to form an outer spacer on a sidewall of the gate pattern and to form a blocking oxide layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

etching the silicon nitride layer using the outer spacer and the blocking oxide layer as an etch mask to form an inner spacer interposed between the outer spacer and the gate pattern and to form a blocking nitride layer under the blocking oxide layer.

10. (Withdrawn) The method of claim 5, wherein forming the spacer insulation layer comprises:

forming a silicon nitride layer on the semiconductor substrate, wherein the first region comprises the silicon nitride layer; and

conformally forming a silicon oxide layer on the silicon nitride layer.

11. (Withdrawn) The method of claim 10, wherein anisotropically etching the spacer insulation layer comprises:

anisotropically etching the silicon oxide layer to form an outer spacer on the sidewall of the gate pattern; and

etching the silicon nitride layer using the outer spacer as an etch mask to form a blocking nitride layer on the isolation layer and on a portion of the active region neighboring the isolation layer.

12. (Withdrawn) The method of claim 5, wherein anisotropically etching the spacer insulation layer comprises:

etching the spacer insulation layer on the active region neighboring the gate pattern is etched at a faster rate than the spacer insulation layer on the active region neighboring the field insulation layer.

13. (Currently amended) A semiconductor device comprising:

an isolation layer disposed in a semiconductor substrate, the isolation layer defining-an active region, the isolation layer including an indentation in a region neighboring the active region;

a gate pattern disposed on the active region;

source/drain regions disposed in the active region at both sides of the gate pattern;

sidewall spacers disposed on sidewalls of the gate pattern;

a blocking insulation layer disposed on the isolation layer, the indentation, and on a portion of the active region neighboring the indentation; and

a first silicide layer disposed on one of the source/drain regions between the blocking insulation layer and one of the sidewall spacers and having a boundary aligned to an edge[[s]] of the blocking insulation layer and an edge of one of the sidewall spacers.

14. (Previously presented) The semiconductor device of claim 13, wherein the sidewall spacer comprises:

an inner spacer having an L-shaped cross-section that is formed on the sidewall of the gate pattern and on the active region neighboring the gate pattern; and

an outer spacer having a curved sidewall that is formed on the inner spacer.

15. (Previously presented) The semiconductor device of claim 13, further comprising a second silicide layer disposed on a top surface of the gate pattern.

16. (New) The semiconductor device of claim 1, wherein a slope of a surface of the blocking insulation layer immediately above the edge of the blocking insulation layer is less than a slope of a surface of the one of the sidewall spacers immediately above the edge of the one of the sidewall spacers.

17. (New) The semiconductor device of claim 1, further comprising silicon nitride material disposed between the blocking insulation layer and the isolation layer.

18. (New) The semiconductor device of claim 13, wherein a thickness of a portion of the blocking insulation layer disposed on the isolation layer is greater than a thickness of a portion of the blocking insulation layer at the edge of the blocking insulation layer.

19. (New) The semiconductor device of claim 13, wherein a slope of a surface of the blocking insulation layer immediately above the edge of the blocking insulation layer is less than a slope of a surface of the one of the sidewall spacers immediately above the edge of the one of the sidewall spacers.

20. (New) The semiconductor device of claim 13, further comprising silicon nitride material disposed on the isolation layer, the indentation, and on the portion of the active region neighboring the indentation, wherein the silicon nitride material is below the blocking insulation layer.

21. (New) The semiconductor device of claim 13, wherein the blocking insulation layer fills the indentation.

22. (New) The semiconductor device of claim 1, wherein a thickness of a portion of the blocking insulation layer disposed on the isolation layer is greater than a thickness of a portion of the blocking insulation layer at the edge of the blocking insulation layer.